C-MOS Gate-Array TS240

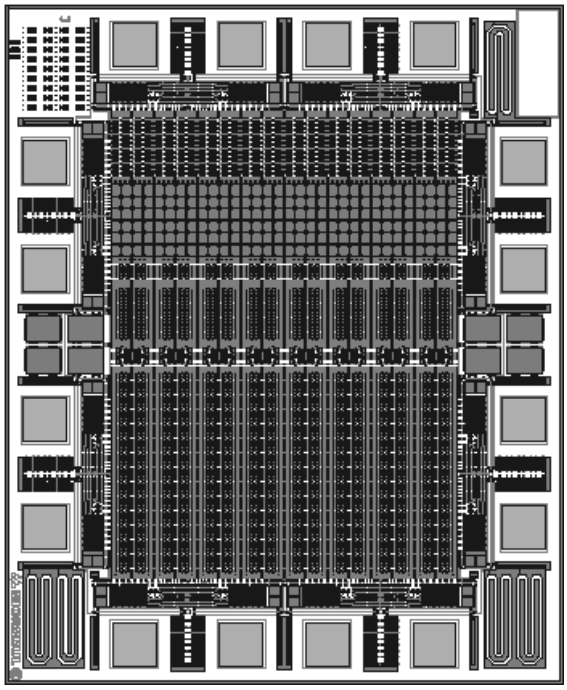
DESCRIPTION

The TS240 is a semicustom masterchip built in a double metal C-MOS technology. The main application of this component array is to realize mixed-signal ASICs (Application Specific Integrated Circuits) of moderate complexity in a rather short development time and with low development costs. The chip contains a lot of different active and passive components which can be interconnected by two customized metal masks and a via mask. The larger part of the TS240 has a gate-array structure which is mainly used for digital circuits. In addition to the gate array part, it contains an analog section with transistors of different sizes, diodes, resistors and capacitors. This part can be used to realize numerous analog functions. Finally, a third part contains a 32 bits EPROM cell which allows to adjust electrically some parameters. The available components and the low threshold voltage of the employed C-MOS process make the TS240 specially suited to build low current and low voltage circuits.

FEATURES

- Digital part: 2'400 transistor pairs (N-MOS and P-MOS)
- Analog part: Separate N-MOS and P-MOS transistors, diodes, low and high value resistors, floating capacitors
- 16 input/output cells
- 32 bits EPROM
- Programmable by two metal masks and one via mask. Very flexible wiring possibilities
- Processed with the proven C175SC technology of PHILIPS SEMICONDUCTORS
- Supply voltage range: 0.9V to 9.0V
- High speed operation: min. 100MHz toggle frequency at V_{DD} = 4.5V
- Small chip size: 1.20mm x 1.44mm Encapsulation in SO8 package possible

LAYOUT



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SHORT PROCESS DESCRIPTION

- N-well silicon-gate C-MOS process. PHILIPS process code: C175SC
- Low threshold voltage: V_{TN} = 0.60V ± 0.15V, V_{TP} = 0.80V ± 0.15V
- Gate oxyde: 17.5nm, 1.97fF/µm^2
- Nominal gate length: $Leff_N$ = 0.85µm, $Leff_P$ = 1.0µm
- Operating voltage range: 0.9V to 9V
- 2 metal layers, 1 polysilicon layer
- Floating capacitor between metal1 and polysilicon: 0.85fF/µm^2
- Polysilicon: Width 1.0µm Pitch 2.4µm Sheet resistance 30Ω/square
  Metal1: Width 1.2µm Pitch 2.4µm Sheet resistance 60mΩ/square
  Metal2: Width 1.2µm Pitch 2.4µm Sheet resistance 35mΩ/square
- Contact holes: 0.6µm x 0.6µm, vias: 0.8µm x 0.8µm
- P-substrate (0.01Ωcm) with p-epitaxial layer 12µm (10Ωcm)
- Number of masks: 13
- Number of custom masks: 3

DIGITAL PART

- 2'208 transistor pairs standard sized (N: 6.0/1 P: 8.4/1)
- 128 transistor pairs with small dimensions (N: 2.4/1 P: 2.4/1) specially suited for lower current frequency dividers
- 64 transistor pairs with adapted dimensions (N: 6.0/1 P: 2.4/1) specially suited for level shifters
- 32 bits EPROM specially interesting to electrically adjust some analog parameters
- 16 input/output cells
- The basic transistor pairs can be connected with the metal mask into NOR and NAND gates with any number of inputs, into transmission gates, combined logic functions, latches, flip-flops, etc.

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ANALOG PART

MOS TRANSISTORS

Size	Width (µm)	Length (µm)	Number
NA	6.0	5.6	384
PA	6.0	5.6	384

The transistors of size NA and PA are mainly used for amplifiers and comparators. The 5.6µm gate length results in a lower offset voltage and higher gain fo the amplifier than the standard 1µm gate lenth.
The N-well of the P-MOS is divided into several isolated regions, allowing an optimum circuit design in case of different supply voltages (e.g. for voltage doublers, separate LCD supply, etc.).

DIODES

39 single emitter bipolar PNP substrate transistors are provided. They are mainly foreseen for temperature compensated bandgap voltage references. Their small emitter area of 4.8µm x 16.8µm provides a higher current density for low power applications.

RESISTORS

Value (Ω)	Number	Tolerance (%)	TC (%/°C)
800	384	-30 +30	0.06
2250	16	-30 +30	0.06
55k	48	-10 +10	0.53
275k	23	-10 +10	0.53

CAPACITORS

	Size 1	Size 2
Maximum capacitance	0.32pF	9.8pF
Substrate capacitance (typ.)	0.03pF	1pF
Number of areas	192	8

The floating capacitors of size 1 are built between the polysilicon and the metal1, in areas where the polysilicon is covered only by a thin oxyde layer which results in a high specific capacitance.
The floating capacitors of size 1 are built as a sandwich. A floating part between metal1 and polysilicon has a value of 2.8pF and the oter part is a gate to substrate capacitance of 7pF.

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PERIPHERY

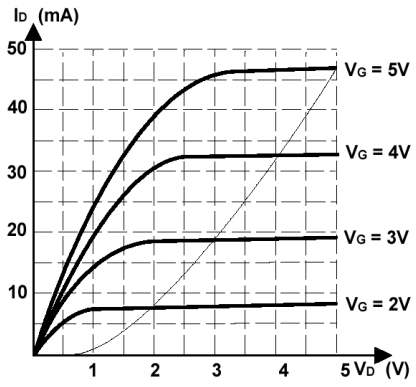
The periphery consists of 16 identical cells containing one pad, two buffer transistors (1 N-MOS and 1 P-MOS) and two 60kΩ pullup/pulldown resistors. Each cell is programmable as supply, as input, as push-pull output, as open-drain output or as bidirectional I/O pin. The output transistors can also be connected as transmission gates. The transistors of adjacent cells can be connected together to increase the output drive capability.

An electrostatic discharge (ESD) structure which protects the pin against overvoltage is also part of each periphery cell. This structure sustain ESD test pulses of more than 2kV (Generator impedance: 100pF, 1.5kΩ)

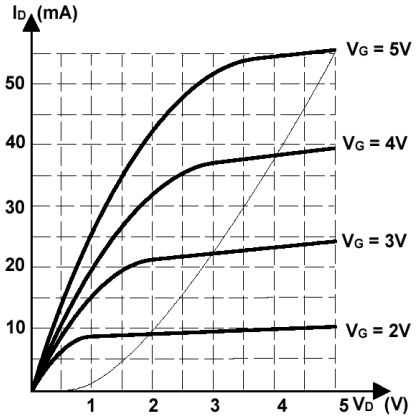
Size of the output transistors:	N-Buffer	203µm / 2.0µm
	P-Buffer	422µm / 1.2µm

Typical characteristics of the output transistors

N-Buffer



P-Buffer



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